In making the various references to the specifications and drawings set forth herein, it is to be understood that Applicants are in no way intending to limit the scope of the claims to the exemplary embodiments shown in the drawings and described in the specification. Rather, Applicants expressly affirm that they are entitled to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation, and applicable case law.

In the outstanding Office Action, the Examiner rejected claims 14, 18, 22, 27, 32 and 33 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as the invention; rejected claims 14-31 under 35 U.S.C. § 103(a) as being unpatentable over Shin (U.S. Patent No. 5,270,257) and Kirvokapic (U.S. Patent No. 6,025,635); and rejected claims 32-33 under 35 U.S.C. § 103(a) as being unpatentable over Shin, Kirvokapic, and Lee (U.S. Patent No. 6,228,763).

Applicants note that in the present Office Action the Examiner has not provided a proper statutory basis for the rejections set forth under 35 U.S.C. § 103(a). See M.P.E.P. § 707.07(d). Instead, individual elements of Applicants' claims have been alleged to have been taught by the cited references. For example, for claims 32 and 33, the Office Action merely alleges that specific elements of the claims are taught by Shin, Kirvokapic, and Lee without any indication of the legal basis for the Examiner's conclusion of obviousness. In view of the improper rejection set forth in the outstanding Office Action, Applicants request that any subsequent rejection of the claims be made non-final and that Applicants be advised of the proper statutory basis for the rejection so that they may respond as appropriate.

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With the intention of being fully responsive to the Office Action, Applicants respectfully request reconsideration of the application based on the following remarks:

Rejection under § 112, second paragraph

Regarding the rejection under 35 U.S.C. § 112, second paragraph, the Examiner rejected claims 14,18, 22, 27, 32, and 33, as being indefinite because of the phrase "including a part of a bottom of said first groove."

Applicants have amended claims 14 and 18 to replace the phrase "of a bottom said groove" with "thereof extending below the first groove," as suggested by the Examiner. Accordingly, Applicants request the Examiner to withdraw the rejection of claims 14 and 18 under 35 U.S.C. § 112, second paragraph.

Regarding claims 22, 27, 32, and 33, Applicants point out that the rejection under 35 U.S.C. § 112, second paragraph, is improper because these claims do not include the recitation "including a part of a bottom of said first groove," as alleged to by the Examiner. Therefore, Applicants respectfully request that the Examiner withdraw the rejection of claims 22, 27, 32, and 33 under 35 U.S.C. § 112, second paragraph.

Rejection under § 103(a)

In the Office Action, the Examiner rejected claims 14-31 under 35 U.S.C. § 103(a) as being unpatentable over Shin (U.S. Patent No. 5,270,257) further in view of Kirvokapic (U.S. Patent No. 6,025,635); and rejected claims 32-33 under 35 U.S.C. § 103(a) as being unpatentable over Shin, Kirvokapic, and Lee.

Regarding the 35 U.S.C. § 103(a) rejection of claims 14-33, Applicants respectfully disagree with the Examiner's arguments and conclusions as set forth in the Office Action.

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To establish a *prima facie* case of obviousness under 35 U.S.C. §103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. (See M.P.E.P. §2143.03 (8th ed. 2001)). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." (M.P.E.P. §2143 (8th ed. 2001)).

The Examiner further states in the "Response to Arguments" section of the Office Action that "Applicants' arguments are based on attacking the references individually whereas the rejection is based on the combined teachings of Shin and Kirvokapic." Office Action at page 7. However, the Examiner has mischaracterized the arguments presented in the previous response; namely, that Shin and Kirvokapic, either taken alone or *in combination*, do not teach each and every element of the rejected claims 14-31; and Shin, Kirvokapic, and Lee, either taken alone or *in combination*, do not teach each and every element of the rejected claims 32-33.

I. Claims 14 and 18

The Examiner's rejection of claims 14 and 18 under § 103 fails to meet the essential requirements for a *prima facie* case of obviousness, as set forth below.

Claim 14 and 18 recite a method for producing a MIS transistor comprising, *inter alia*, forming an insulator film on an impurity diffusion region and thereafter removing a second film to form a second groove in the semiconductor substrate.

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In contrast, Shin discloses in Figs. 3a and 3b forming a nitride layer 22 on a substrate 21, etching a portion of the nitride layer 22 to form a mask, and then etching the substrate 21 to form a trench (col. 4, lines 15-27). Fig. 3b further shows a gate oxide layer 23 is grown on the exposed trench surface of the substrate 21 and the nitride layer 22 (col. 4, lines 30-32). A polysilicon gate 24 is formed in the trench, and the silicon substrate 21 is doped to form source 26a and drain 26b (Fig. 3b, col. 4, lines 40-47).

Fig. 3b of Shin shows a gate oxide layer 23, which is grown on the exposed trench surface of the substrate; however, Shin does not teach or suggest at least forming an insulator film on an impurity diffusion region and thereafter removing a second film to form a second groove in the semiconductor substrate, as recited in claims 14 and 18. In fact, the gate oxide film 23 (alleged by the Examiner to read on the claimed "second film") is not removed at all. Furthermore, nothing in Shin discloses forming a second groove, or a second groove in the semiconductor substrate.

Therefore, Shin does not teach or suggest all the elements of claims 14 and 18, for example, forming an insulator film on an impurity diffusion region and thereafter removing a second film to form a second groove in the semiconductor substrate, as recited in claims 14 and 18.

See 1/A page

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Krivokapic does not cure the deficiencies of Shin noted above. Contrary to the allegations of the Examiner, Figs. 8, 9, and 15 of Krivokapic do not teach or suggest at least forming an insulator film on an impurity diffusion region and thereafter removing a second film to form a second groove in the semiconductor substrate, as recited in claims 14 and 18.

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Fig. 8 of Krivokapic discloses forming adaptively controlled spacers 215 in gate region 190 (col. 6, lines 19-21) by depositing Si_3N_4 and isotopically etching the Si_3N_4 layer to yield spacers 215. Id. at col. 6, lines 19-24. Fig. 9 discloses etching oxide layer 200 to leave a minor portion of the oxide layer 200a under spacers 215 for support. Id. at col. 6, lines 28-34.

First, while Krivokapic discloses etching oxide layer 200 to leave a minor portion 200a under spacers for support, it does not teach or suggest at least forming an insulator film on an impurity diffusion region and thereafter removing a second film *to form a second groove in the semiconductor substrate*, as claimed. The "second groove" is formed on *top* of the substrate 60. See Figs. 8 and 9. Second, Figs. 8 and 9 of Krivokapic do not disclose that the oxide layer 200 is formed *on an impurity region*, as recited in claims 14 and 18.

Fig. 13 of Krivokapic discloses the device after formation of a source and drain region, which are formed by a deposition or implantation of an impurity. Id. at col. 7, lines 7-12. While Fig. 15 of Krivokapic discloses a film 232 on an impurity region 200a, film 232 is NOT removed. Therefore, in reference to film 232, Krivokapic does not disclose the step of "thereafter removing a second film to form a second groove in the semiconductor substrate," as claimed. Furthermore, both films 200 and 232 are formed on the *surface* of the substrate 60 and therefore, it is impossible to create any groove *in the semiconductor substrate* by their removal.

Thus, neither the film 200 nor the film 232 (nor any other film) of Krivokapic cure the deficiencies of Shin. To summarize Shin and Kirvokapic, either taken alone *or in combination*, do not teach or suggest at least "forming an insulator film on said impurity

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region and thereafter removing said second film to form a second groove in the semiconductor substrate," as recited in claims 14 and 18. Likewise, there is lack of any reasonable expectation of success from combining the references.

Furthermore, Applicants respectfully disagree with the Examiner's allegations that it would have been obvious for of ordinary skill in the art at the time of the invention to include the steps of Kirvokapic. Specifically, it would be inconsistent to include the teachings of Kirvokapic in the steps of making a MOSFET disclosed in Shin. As an example, if the Examiner alleges that the gate oxide film 23 of Shin reads on the claimed "second film," and relies on Kirvokapic to teach the claimed step of "thereafter removing said second film to form a second groove in the semiconductor substrate," it would yield an undesirable instance of having an exposed region of the semiconductor substrate before the step of ion-injection to make the source and drain regions. See id. at col. 4, lines 30-54 and Fig. 2b.

Finally, even if a motivation stemming from an alleged general desire to make more efficient devices were a sufficient reason to combine references (which, it is not), it is improper to rely on such general motivation to pick and choose at random elements from one reference to cure the deficiencies of another reference. Without appropriate particularized motivation from the references themselves or from knowledge generally known in the art to combine specific elements of one reference with the elements of another reference, the Examiner is, in effect, ignoring the Applicants' invention by inappropriately using the present application's own teachings as motivation to modify the cited references. To do this, constitutes impermissible hindsight based on Applicants' disclosure.

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To summarize, the Examiner has failed to make a *prima facie* case of obviousness at least because Shin and Krivokapic, either taken alone or in combination, do not teach each and every element of claims 14 and 18. Therefore, Applicants respectfully request that the Examiner withdraw the rejection of claims 14 and 18 under 35 U.S.C. § 103(a), and the claimed be allowed.

Claims 15-17 and 19-21 depend from claim 14 and 18, respectively. Accordingly, these claims are allowable as well at least in view of their dependency from allowable claims 14 and 18.

I. Claims 22 and 27

The Examiner's rejection of claims 22 and 27 under § 103 fails to meet the essential requirements for a *prima facie* case of obviousness, as set forth below.

Claim 22 recites a method for producing a MIS transistor comprising, *inter alia*, removing a first film so as to form a groove in the semiconductor substrate; and forming a gate insulator in the groove in the semiconductor substrate so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region.

As shown in Fig. 3c of Shin, a bottom surface of source 26a and drain 26b is higher than the bottom surface of the trench. Fig. 3b further shows a gate oxide layer 23 is grown on the exposed trench surface of the substrate 21 As is clear from Figs. 3b and 3c, to the extent source 26a or drain 26b may correspond to the impurity diffusion region, Shin does not teach or suggest at least forming a gate insulator in the groove in the semiconductor substrate so that a top surface of said gate insulator film is higher than a top surface of an impurity diffusion region, as claimed.

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Krivokapic fails to cure the above-mentioned deficiencies of Shin. As mentioned before with respect to claims 14 and 18, Fig. 15 of Krivokapic discloses a film 232 on an impurity region 200a. However, Krivokapic does not teach or suggest at least forming a gate insulator in the groove in the semiconductor substrate so that a top surface of said gate insulator film is higher than a top surface of an impurity diffusion region, as claimed. In fact, film 232 is formed on the *surface* of the substrate 60 and therefore, it is impossible to be in a *groove in the semiconductor substrate*.

Therefore, Shin and Kirvokapic, either taken alone or in combination, do not teach or suggest at least removing a first film so as to form a groove in the semiconductor substrate; and forming a gate insulator in the groove in the semiconductor substrate so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region, as claimed.

Claim 27 recites a method for producing a MIS transistor comprising, *inter alia*, forming an insulator film on said impurity diffusion region; removing a first film so as to form a groove in the semiconductor substrate; and forming a gate insulator in said groove in the semiconductor substrate and on said insulator film.

As shown in Figs 3b and 3c, Shin discloses a gate oxide layer 23 is grown on the exposed trench surface of the substrate 21 and the nitride layer 22 (col. 4, lines 30-32). A polysilicon gate 24 is formed in the trench, and the silicon substrate 21 is doped to form source 26a and drain 26b. Id. at col. 4, lines 40-47. However, Shin does not teach or suggest at least forming an insulator film on said impurity diffusion region; removing a first film so as to form a groove in the semiconductor substrate; and forming a gate

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insulator in said groove in the semiconductor substrate and on said insulator film, as claimed.

Krivokapic fails to cure the above-mentioned deficiencies of Shin for the reasons set forth above, namely, that the films disclosed in Kirvokapic are formed on the *surface* of the substrate 60 and therefore, it is impossible for them to be in a *groove in the semiconductor substrate*.

Therefore, Shin and Kirvokapic, either taken alone or in combination, do not teach or suggest at least forming an insulator film on said impurity diffusion region; removing a first film so as to form a groove in the semiconductor substrate; and forming a gate insulator in said groove in the semiconductor substrate and on said insulator film, as claimed.

Accordingly, the Examiner has failed to make a *prima facie* case of obviousness for claims 22 and 27 and Applicants respectfully request the Examiner to withdraw the rejection of claims 22 and 27 under 35 U.S.C. § 103(a), and the claims be allowed.

Claims 23-26 and 28-31 depend from claim 22 and 27, respectively. Accordingly, these claims are allowable as well at least in view of their dependency from allowable claims 22 and 27.

III. Claim 32

Claim 32 recites a method for producing a MIS transistor comprising, *inter alia*, selectively depositing semiconductor layers serving as said source/drain regions so that an inclined surface is formed between the top surface of said semiconductor substrate and said channel region.

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With respect to claim 32, none of the cited references disclose or suggest "selectively depositing semiconductor layers serving as said source/drain regions so that an inclined surface is formed between the top surface of said semiconductor substrate and said channel region." All the features shown in Shin consists of flat substrates. The Examiner alleges Fig. 13 of Kirvokapic shows the claimed feature since the rejection is based on the combined teachings of Shin and Kirvokapic. See Office Action at page 10. However, Applicants fail to see any inclined surface between the top surface of the semiconductor substrate and a channel region. In fact, the whole top surface of the structure disclosed in Fig. 13 (consisting of the source and drain regions 200a and the first and second implant regions, 225 and 230, respectively) is completely flat.

Lee, cited only for the T-shaped cross-section, does not cure the deficiencies of the Shin and Kirvokapic combination. Therefore, Shin, Kirvokapic, and Lee, either taken alone or in combination, do not teach or suggest at least selectively depositing semiconductor layers serving as said source/drain regions so that an inclined surface is formed between the top surface of said semiconductor substrate and said channel region, as claimed.

Therefore, the Examiner has failed to make a *prima facie* case of obviousness for claim 32 and Applicants respectfully request the Examiner to withdraw the rejection of claim 32 under 35 U.S.C. § 103(a), and the claim be allowed.

Claim 33 depends from claim 32. Accordingly, claim 32 is also allowable at least in view of its dependency from allowable claim 32.

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Conclusion

In view of the foregoing remarks, Applicant requests the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: April 23, 2003

By: Reg 24,014
Richard V. Burgujian
for Reg. No. 31,744

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APPENDIX TO AMENDMENT OF APRIL 23, 2003

Version with markings to show the changes made

In the claims:

Please amend claims 14, 18, 22, and 27, as follows:

14. (Twice Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the semiconductor substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

etching said semiconductor substrate to form a first groove by using said first film as a mask;

forming a second film in said first groove and thereafter removing said first film;

diffusing an impurity on a surface of said semiconductor substrate to form an impurity diffusion region including a part [of a bottom of said] thereof extending below the first groove by using said second film as a mask;

forming an insulator film on said impurity diffusion region and thereafter removing said second film to form a second groove in the semiconductor substrate;

forming a gate insulator film in said second groove so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region; and

forming a gate electrode on the top surface of said gate insulator film.

18. (Twice Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the semiconductor substrate,

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and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

etching said semiconductor substrate to form a first groove by using said first film as a mask;

forming a second film in said first groove and thereafter removing said first film;

diffusing an impurity on a surface of said semiconductor substrate to form an impurity diffusion region including a part [of a bottom of said] thereof extending below the first groove by using said second film as a mask;

forming an insulator film on said impurity diffusion region and thereafter removing said second film to form a second groove in the semiconductor substrate;

forming a gate insulator film in said second groove and on said insulator film;

polishing said gate insulator film by using said insulator film as a stopper so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region; and

forming a gate electrode on the top surface of said gate insulator film.

22. (Twice Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

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diffusing an impurity on a surface of said semiconductor substrate to form an impurity diffusion region including an elevated impurity diffusion region from a channel region by using said first film as a mask;

forming an insulator film on said impurity diffusion region;

removing said first film so as to form a groove in the semiconductor substrate;

forming a gate insulator in said groove in the semiconductor substrate so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region; and

forming a gate electrode on a top surface of said gate insulator film.

27. (Twice Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

diffusing an impurity on a surface of said semiconductor substrate to form an impurity diffusion region including an elevated impurity diffusion region from a channel region by using said first film as a mask;

forming an insulator film on said impurity diffusion region;

removing said first film so as to form a groove in the semiconductor substrate;

forming a gate insulator in said groove in the semiconductor substrate and on said insulator film;

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polishing said gate insulator film by using said insulator film as a stopper so that a top surface of said gate insulator film is higher than a top surface of said grooved impurity diffusion region; and

forming a gate electrode on a top surface of said gate insulator film.

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